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10/775,521	02/09/2004	Sam Nemazie	SiliconStor-02US	1050

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EXAMINER	
LEE, CHUN KUAN	
ART UNIT	**PAPER NUMBER**
2181	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/775,521	NEMAZIE, SAM	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 4-43* is/are rejected.

7)☒ Claim(s) *20,21,33 and 34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *01/19/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

RESPONSE TO ARGUMENTS

1. Applicant's arguments with respect to claims 1 and 4-43 have been considered but are moot in view of the new ground(s) of rejection. Currently, claims 2-3 are canceled and claims 1 and 4-43 are pending for examination.

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

II. INFORMATION CONCERNING DRAWINGS

Drawings

3. The applicant's drawings submitted are acceptable for examination purposes.

III. ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

4. As required by **M.P.E.P. 609(C)**, the applicant's submissions of the Information Disclosure Statement dated January 19, 2007 is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

IV. OBJECTIONS TO THE CLAIMS

Claim Objections

5. Claims 20-21 and 33-34 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

As per claims 20 and 33, it appears the independent claims 18 and 31 which claims 20 and 33 respectively dependent on already include the claimed limitations recited in claims 20 and 33; more specifically, the examiner is referring to the claimed limitation "first serial ATA port includes a first host task file."

As per claims 21 and 34, it appears the independent claims 18 and 31 which claims 21 and 34 respectively dependent on already include the claimed limitations recited in claims 21 and 34; more specifically, the examiner is referring to the claimed limitation "second serial ATA port includes a second host task file."

V. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 4, 6-14 and 18-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grieff et al. (US Patent 6,961,813) in view of "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Utsunomiya et al. (US Pub.: 2003/0131166).

7. As per claims 1, 18, 20-21, 31 and 33-34, Grieff teaches a switch coupled between a plurality of host units and a device via serial advanced technology attachment (SATA) for communicating there between and said switch comprising:

a) a first SATA port (Fig. 1, ref. 130) for connection to a first host unit, said first port for causing access, to the device, by the first host unit (col. 3, ll. 13-24 and col. 5, l.17 to col. 7, l. 6);

b) a second SATA port (Fig. 1, ref. 132) for connection to a second host unit, said second port for causing access to the device, by the second host unit (col. 3, ll. 13-24 and col. 5, l.17 to col. 7, l. 6);

c) a third SATA port (device-side link layer on Fig. 1) for connection to a device, for causing access to the device, by the first or second host units (col. 3, ll. 13-24 and col. 5, l.17 to col. 7, l. 6);

d) an arbitration and control circuit (arbiter module 112 and switch 110 of Fig. 1), coupled to the first, second and third ports, for selecting one of the first host unit or the second host unit to be coupled to the device, through the switch (col. 3, ll. 13-24 and col. 5, l.17 to col. 7, l. 6); and

wherein the switch enable multiple hosts to share access to the device (e.g. single ATA device) (col. 3, ll. 14-16), such that the device can maintain communication with the multiple hosts (col. 3, ll. 43-45); and

wherein the switch includes a buffer that allows the first host to post a single, non-queue command if the second host currently has outstanding queued commands (col. 5, ll. 36-39).

Grieff does not expressly teach the switch comprising:

wherein the first SATA port includes a first host task file that is responsive to commands sent by the first host unit;

wherein the second SATA port includes a second host task file that is responsive to commands sent by the second host unit;

wherein the third port is a PATA port;

selecting one of the first host or the second host units to concurrently access the device by accepting commands, from either of the first or the second host units, at any given time, including when the deice is not in an idle state.

"SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" teaches the utilization of PATA ("SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", pages 1-2).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA's utilization of the PATA into Grieff's switch. The resulting combination of the

references teaches the switch comprising of a third PATA port connecting to a peripheral device.

Therefore, it would have been obvious to combine "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" with Grieff for the benefit of having a peripheral port that is backward comparable allowing users to be able to connecting existing PATA peripheral devices instead of purchasing new peripheral devices that conform to the new SATA standard.

Utsunomiya teaches a system and a method comprising:

a host computer issuing a plurality of commands to the drive apparatus (Fig. 3, ref. 12) at the same time (e.g. concurrently), wherein the drive apparatus operates in accordance to ATA ([0004] and [0007]);

a command queue including a task file queue enabling the host computer to issue the plurality of commands to be processed by the drive apparatus at the same time (e.g. concurrently), as the task file queue storing the plurality of commands ([0005]-[0008] and [0020]-[0024]), therefore the task file queue would enable the host computer to issue the plurality of commands, at any given time, even when the drive apparatus is in a busy status ([0005]); and

wherein the plurality of commands issued by the host computer are transferred from the task file queue to the drive apparatus' task file (Fig. 5 and [0022]).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Utsunomiya's task file queue into Grieff and SATA vs.

PATA: the reality of Serial and Parallel ATA - Serial ATA's ATA ports. The resulting combination of the references further teaches the switch comprising:

wherein the first SATA port includes the first task file queue (i.e. first host task file) storing the plurality of commands issued and sent by the first host unit;

wherein the second SATA port includes the second task file queue (i.e. second host task file) storing the plurality of commands issued and sent by the second host unit; and

wherein the switch selects either the first host unit or the second host unit to concurrently access the drive apparatus (i.e. device) as the switch receives and accepts the plurality of commands, issued by either the first host unit or the second host unit, at any give time, including when the device is in the busy status (i.e. not in an idle state), as the plurality of commands are respectively stored into the first task file queue and the second task file queue.

Therefore, it would have been obvious to combine Utsunomiya with Grieff and SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA for the benefit of decreasing the work load of the host unit for issuing commands (Utsunomiya, [0009]).

8. As per claims 4, 22 and 35, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Utsunomiya teach all the limitation of claims 1, 18 and 31 as discussed above, where Utsunomiya further teaches the switch comprising wherein said third parallel ATA port includes a device task file (Utsunomiya, Fig. 5 and [0022]).

9. As per claims 6, 23 and 36, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Utsunomiya teach all the limitation of claims 1, 18 and 31 as discussed above, where Grieff further teaches the switch comprising wherein said device is a storage unit (Grieff, col. 15, ll. 9-22).

10. As per claims 7, 24 and 37, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Utsunomiya teach all the limitation of claims 1, 18 and 31 as discussed above, where Grieff further teaches the switch comprising wherein said switch is employed in an enterprise system (Grieff, col. 15, ll. 9-22).

11. As per claims 8, 25 and 38, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Utsunomiya teach all the limitation of claims 1, 18 and 31 as discussed above, where Utsunomiya further teaches the switch wherein said arbitration and control circuit causes concurrent access of the device by the first and second host units (Utsunomiya, [0007] and [0020]-[0024]).

12. As per claims 9, 26 and 39, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Utsunomiya teach all the limitation of claims 1, 18 and 31 as discussed above, where Grieff further teaches the switch comprising wherein information, in the form of data, commands or setup, is transferred from the device to the first or second host units through the switch and the information is modified by the

switch prior to being received by the first or second host units such that modified information rather than the information is received by the first or second host units (Grieff, col. 12, l. 60 to col. 14, l. 28).

13. As per claims 10, 27 and 40, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Utsunomiya teach all the limitation of claims 9, 26 and 39 as discussed above, where Grieff further teaches the switch comprising wherein the information is referred to as `identify drive response` (IDENTIFY DEVICE) (Grieff, col. 7, ll. 39-61).

14. As per claims 11, 28 and 41, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Utsunomiya teach all the limitation of claims 9, 26 and 39 as discussed above, where Grieff further teaches the switch comprising wherein the information is referred to as `Tag` (Grieff, col. 12, l. 60 to col. 14, l. 28).

15. As per claims 12, 29 and 42, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Utsunomiya teach all the limitation of claims 1, 18 and 31 as discussed above, where Grieff further teaches the switch comprising wherein information, in the form of data, commands or setup, is transferred from the first or second host units to the device through the switch and the information is modified by the switch prior to being received by the device such that modified information rather

than the information is received by the device (Grieff, col. 5, l. 65 to col. 6, l. 56 and col. 10, l. 27 to col. 11, l. 36).

16. As per claims 13 and 43, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Utsunomiya teach all the limitation of claims 12 and 42 as discussed above, where Grieff further teaches the switch comprising wherein the information is referred to as `Tag` (Grieff, col. 5, l. 65 to col. 6, l. 56 and col. 10, l. 27 to col. 11, l. 36).

17. As per claim 14, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Utsunomiya teach all the limitation of claim 13 as discussed above, where Grieff further teaches the switch comprising wherein the arbitration and control circuit include a Tag/Sactive Mapping Circuit (Grieff, Command Tracker SM 114 of Fig. 1) for mapping the host tag to the device tag and inverse mapping for identifying a host (Grieff, col. 5, l. 65 to col. 6, l. 56; col. 10, l. 27 to col. 11, l. 36 and col. 12, l. 60 to col. 14, l. 28).

18. As per claims 19 and 32, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Utsunomiya teach all the limitation of claims 18 and 31 as discussed above, where Grieff further teaches the switch comprising wherein the switch is a serial ATA switch (Grieff, col. 3, l. 13 to col. 4, l. 4 and col. 5, l. 65 to col. 6, l. 56).

19. As per claim 30, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Utsunomiya teach all the limitation of claim 28 as discussed above, where Grieff further teaches the switch comprising wherein the information is referred to as `Tag` (Grieff, col. 5, l. 65 to col. 6, l. 56 and col. 10, l. 27 to col. 11, l. 36).

20. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Grieff et al. (US Patent 6,961,813), "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Utsunomiya et al. (US Pub.: 2003/0131166) as applied to claims 1, 4, 6-14 and 18-43 above, and further in view of Boucher et al. (US Patent 6,434,620).

Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Utsunomiya teach all the limitations of claim 4 as discussed above, where Utsunomiya further teaches the switch comprising wherein said first, second and third ports include the corresponding task file queue (Fig. 4-5 and [0020]-[0024]).

Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Utsunomiya does not expressly teach the switch comprising wherein said first, second and third ports are level 4 ports.

Boucher teaches a communication interface between a peripheral comprising the intelligent network interface card (INIC 50 of Fig. 1) and a host (Fig. 1, ref. 52) comprising a physical layer communication path (Fig. 1, ref. 57) and two other communication paths at higher communication layer (Fig. 1 and col. 6, l. 60 to col. 7, l. 10).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Boucher's higher layer communication path into Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Utsunomiya's switch. The resulting combination of the references teaches the switch further comprising the ports, interconnection between the hosts and the peripheral device, operating at level 4, as it is well known to one skilled in the art that the highest communication layer for SATA is application layer (level 4).

Therefore, it would have been obvious to combine Boucher with Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Utsunomiya for the benefit of providing a faster communication path between the peripheral device and the host (Boucher, Fig. 1).

21. Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grieff et al. (US Patent 6,961,813) in view of "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Utsunomiya et al. (US Pub.: 2003/0131166), and "Serial ATA Specification".

Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Utsunomiya teach all the limitations of claim 1 as discussed above.

Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Utsunomiya does not expressly teach the switch comprising wherein either the first or the second host sends a legacy queue command queued by the device; and wherein

either the first or the second host sends a native queue command for execution thereof by the device.

"Serial ATA Specification" teaches the utilization of the legacy ATA queuing (legacy queue command) and the native Serial ATA queuing (native queue command) by the Serial ATA device (Section D.1.5 on page 301).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Serial ATA Specification's queuing of legacy queuing command and the execution of the native queuing command into Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Utsunomiya's switch.

Therefore, it would have been obvious to combine Serial ATA Specification with Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Utsunomiya for the benefit of because Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Utsunomiya's storage device conforms to the Serial ATA standard, therefore enable backward compatibility to prior technology standard and improve performance by enabling multiple commands to be outstanding within the SATA device at the same time.

22. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Grieff et al. (US Patent 6,961,813) in view of "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Utsunomiya et al. (US Pub.: 2003/0131166), and Shin et al. (US Patent 7,154,905).

Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Utsunomiya teach all the limitations of claim 1 as discussed above, where Grieff further teaches the switch comprising:

wherein said first, second and third ports are operating at link layer (level 2 ports) (Grieff, Fig. 1); and

a Data FIS FIFO (Grieff, host FIS buffer 120 and device FIS buffer 122 of Fig. 1) and an associated FIFO Control (Grieff, Command Tracker SM 114 of Fig. 1) are coupled to the first, second and third ports and are located externally thereto (Grieff, Fig. 1 and col. 5, l. 65 to col. 6, l. 56).

Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Utsunomiya does not expressly teach the switch comprising wherein the first, second and third ports are level 3 SATA ports.

Shin teaches the utilization of a port including a transport layer (i.e. level 3 serial ATA port) (Fig. 1; Fig. 38A and col. 2, ll. 26-44).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Shin's transport layer into Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Utsunomiya's ATA ports. The resulting combination of the references teaches the switch coupled between the plurality of host units, further comprising wherein the first, second and third ports are level 3 serial ATA ports.

Therefore, it would have been obvious to combine Shin with Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Utsunomiya for the

benefit of providing a communication architecture that provides high-performance for applications at a low cost (Shin, col. 4, ll. 25-30).

VI. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1 and 4-43 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

IMPORTANT NOTE

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

February 28, 2007

Chun-Kuan (Mike) Lee
Examiner
Art Unit 2181

DONALD SPARKS
SUPERVISORY PATENT EXAMINER